

Metamor BUFG assignments and the X84 VHDL divider example

Description: This ap note describes an XNFPREP error which can occur when re compiling the X84div.vhd program which ships with the X84 FPGA kits from APS. The error has to do with the Metamor compiler automatically assigning BUFG to signals which are used as clocks. Several solutions are suggested. One which we recommend involves setting the Metamor compile option which controls this

PROBLEM:

When routing the compiler X84div.XNF file from the following XACT error occurs:

```
> > XNFPREP: ERROR 4524:
> > The LOC parameter on global buffer `n4u'
(type = BUFG, output signal
> > = n4u) has an invalid value `P24'.
> >
> > The valid LOC values for global buffers
are:
> > TL, TR, BR, BL.
> >
```

SOLUTION:

This problem is caused because the METAMOR VHDL compiler is set to automatically generate BUFG (internal GLOBAL Buffers) Using the automatic buffer assignment the compiler assigns any SIGNAL it sees as a clock to a BUFG. This is great, except that the BUFG inputs can only comes from certain pins. If we want to use a different pin for a clock, and assign a pin attribute other than a qualified BUFGpin then the XNF file generates the following code:

```
SYM, p0, BUFG,LOC=P24, LIBVER=2.0.0
PIN, I, I, The555In
PIN, O, O, p0
END
```

As you can see it has assigned P24 as a BUFG. This is not possible since P24 is not ann assigned BUFG pin. It is not mandatory however that all clock signals use a BUFG. They can use an ordinary IBUF. As a matter of fact, one way of fixing the problem is to edit the XNF file after Synthesis and change BUFG to IBUF. This is not the best way however. The best way is to turn off the automatic BUFG assignment in the VHDL compiler. The way to do this described in the SYNTHESIS HELP options in the FOUNDATION SOFTWARE. It says the following:

Compile options are specified from within the OEM

environment in which the Metamor compiler is found. First please refer to documentation of that tool set. In addition compile options may be set from a file named 'metamor.arg' in the current working directory. This allows the user to set the command line arguments directly. Any settings made by the OEM environment will be overridden by settings in the file 'metamor.arg'. For example in metamor.arg you could set the library alias for the IEEE library using (your file path may vary):

```
-I IEEE
C:\metamor\vhdl_lib\ieee.vhd
C:\metamor\vhdl_lib\synopsys.vhd
```

In addition the path to the directory containing the Metamor library files may be overridden by setting this path as the value of the environment variable METAMOR_LIB. The file metamor.arg may contain any of the following options delimited by whitespace or newline. Some options apply only to specific output formats. It helps to set -x to 0 when debugging metamor.arg .

All formats:

Analyze

```
-a
```

Specifies that only analysis be performed. Analysis is VHDL syntax checking, type checking, and static usage checking.

Log File

```
-g <file_name>
```

Writes a copy of the window to a file.

Elaborate

```
-e <entity>
-e <entity(architecture)>
-e <configuration>
```

Specifies the root (top) of the design to be elaborated. Default is the last configuration, or the last architecture of the last entity to be analyzed.

<p><i>Device</i> -d name Overrides part_name attribute</p> <p><i>Verbose</i> -v</p> <p><i>Specifies verbose mode, which causes debug information about register and macrocell inference to be displayed.</i></p> <p><i>Quiet</i> -q</p> <p><i>Quiet, turn off progress messages.</i></p> <p><i>Clock Enable</i> -c</p> <p><i>Enables the inference of register clock enable. Allows synthesis of a clock enable structure, from certain VHDL coding conventions (see ...). Does not change the behavior of the design, but allows the compiler to take advantage of a clock enable if it exists in target hardware.</i></p> <p><i>Reset</i> -r</p> <p><i>Force all registers with preset to use reset. Transforms registers with asynchronous preset into registers with asynchronous reset, the design behavior remains unchanged. Registers with both preset and reset are not transformed.</i></p> <p><i>Library Alias</i> -l <libname> <file_list></p> <p><i>Specifies an alias for a vhdl library, overrides the default mapping of vhdl library name to file name, this allows multiple files to be associated with a single vhdl library. Files must be specified in the order they are analyzed.</i></p> <p><i>Exit strategy</i> -x #</p> <p><i>Window exit strategy 0 , 1, 2.</i></p> <p><i>0 : never close the window at the end of a compile</i></p> <p><i>1 : close the window if there were no compile errors</i></p>	<p><i>2 : always close the window at the end of a compile</i></p> <p><i>Optimize level</i> -z #</p> <p><i>Optimize level 0 thru 5 .</i></p> <p><i>A value of 0 means no optimization effort, a larger value indicated increased optimization effort.</i></p> <p><i>Cupl only:</i> -p #</p> <p><i>Sets maximum PLA product terms, set to zero for FPGAs</i></p> <p><i>-s #</i></p> <p><i>Sets maximum number of PLA inputs</i></p> <p><i>Open Abel 2 only:</i> -l</p> <p><i>Force output inverters on registers</i> -b</p> <p><i>Force no output inverters on registers</i> -p #</p> <p><i>Max product terms</i> -f xblox</p> <p><i>Enable inference of xblox macrocells</i> -f lpm</p> <p><i>Enable inference of LPM macrocells</i> Xnf only: -h</p> <p><i>Hierarchy, no IBUF or OBUF insertion</i> -u #</p> <p><i>Automatic BUFG limit, set to zero for no BUFG</i> -p # <i>Xilinx family 2k,3k,4k,4ke,5k,7k</i></p>
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-f xblox

Enable inference of xblox macrocells

As you can see a file needs to be created called metamor.arg

This particular file only contains one line as follows:

-u 0

Save this as metamor.arg and place in :

/active/projects/x84div directory

Then resynthesize and the new XNF file will say:

```
SYM, p0, IBUF,LOC=P24, LIBVER=2.0.0  
PIN, I, I, The555In  
PIN, O, O, p0  
END
```

Then the routing software will have no problems

NOTE: If you are designing a project which has not had pins assigned yet, it is a nice feature to have the synthesizer assign the pins for you automatically using the BUFGs. In this way you really don't need to know much about the chip pinout. The pins will be selected automatically. For designs where you want the maximum flexibility, I prefer turning off the option and choosing the pins myself. BUFGs can also be assigned within the VHDL code explicitly. All future X84 disks will have the metamor.arg file shipped with the X84DIV project. APS is also developing a windows utility which will automatically set these metamor.arg options and create the file via a windows interface. When this utility becomes available we will post it on the web page.

APS

TECH SUPPORT

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